

## **REMARKS/ARGUMENT**

In an Office Action dated February 18, 2005, Claims 12-18 are allowed, and Claims 2, 4, 6, 8, 9 and 11 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In an amendment dated June 7, 2005, Claims 2, 4, 6, 8, 9 and 11 were amended to be allowable. Rejected Claims 3, 5, 7 and 10 were also amended to depend from allowable claims. Accordingly, Claims 3, 5, 7 and 10 stood in allowable form.

Examiner Corielus contacted Applicants' representative via telephone on September 18, 2006. Examiner mentioned there were a few issues yet to resolved before the application would be allowed.

### **REGARDING CLAIM 6:**

Examiner stated that limitations of Claim 4 were omitted from Claim 6, as amended, and must be included in independent Claim 6 for it to be allowable. By this amendment Claim 6 has been so amended. Accordingly, Claim 6 stands allowable.

### **REGARDING CLAIM 10:**

Examiner stated that Claim 11 must be amended to include all of the limitations of Claim 10. Applicants do not understand this determination since Claim 11, as Claim 11 already contains all of the limitations of original Claims 1 and 10. In an attempt to comply with Examiner's unclear requirement, the original language of Claim 11 has been separated out into its own paragraph. Accordingly, Claim 11 stands allowable.

REGARDING CLAIM 15:

Examiner objected to the term “interleaving data” being in the preamble of Claim 15. Accordingly, the language “for interleaving data” has been deleted from Claim 15. Accordingly, Claim 15 stands allowable.

REGARDING CLAIM 4:

Examiner stated that Claim 4 reads on the admitted prior art of Figures 1, 2A & 2B. Applicants respectfully traverse this determination. Reference to prior art Figure 1 shows that the AAPA discloses a write address generator (102) coupled to a write address of interleaver memory (106) and a read address generator (104) coupled to a read address of interleaver memory (106). Both write address generator (102) and read address generator (104) must operate together for there to be interleaving in the prior art device of Figures 1, 2A & 2B.

In contrast, Claim 4 requires and positively recites, an **inverse interleaving address generator coupled to the write address port**. Thus, the address generator that is coupled to the “write address” of the interleaver memory of Claim 1 is an “inverse interleaving” address generator. The invention of Claim 4 does require a read address generator be coupled to a read address of the interleaver memory. Accordingly, the AAPA does not teach or suggest all of the limitations of Claim 4. Accordingly, Claim 4 stands allowable in its present form.

REGARDING CLAIM 17:

Examiner stated that Claim 17 reads on the admitted prior art of Figures 1, 2A & 2B. In response thereto, Claim 17 has been amended to further distinguish the functionality of

the claim over that of the AAPA. More particularly, Claim 17 has been amended as follows: “performing a **write** address mapping function that takes an original row address ( $A_{OR}$ ) and transfer number (TN) and provides a new row address ( $A_n$ ) to the memory . . .”. In contrast, the AAPA requires both the write address and read address mapping functions to accomplish this objective. Accordingly, the AAPA does not teach or suggest all of the limitations of Claim 17, as amended. Claim 17 stands allowable.

NEW CLAIM 24:

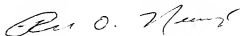
New Claim 24 requires and positively recites a modulator as defined in claim 4, further comprising: a contiguous read address generator coupled to the read address port. While the AAPA discloses a read address generator coupled to the read address port, reference to Figures 2A and 2B clearly discloses that read address generator 104 is NOT a contiguous read address generator. As such, Claim 24 stands allowable over the AAPA.

NEW CLAIM 25:

New independent Claim 25 requires and positively recites, a modulator circuit, comprising: “a memory for storing interleaved data, the memory having a write address port”, “an inverse interleaving address generator coupled to the write address port” and “**a contiguous read address generator coupled to the read address port**”. New independent Claim 25 is original Claim 1 with the added limitation of “**a contiguous read address generator coupled to the read address port**”, which is not taught or suggested by the Fimoff et al. reference. As such, Claim 25 stands allowable.

Claims 12-18 stand allowed. Claims 2-11 and 19-25 stand allowable. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



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